ABSTRACT

An integrated circuit (IC) chip, mounted on a leadframe, has a network of power distribution lines deposited on the surface of the chip so that these lines are located over active components of the IC, connected vertically by metal-filled vias to selected active components below the lines, and also by conductors to segments of the leadframe. Furthermore, the lines are fabricated with a sheet resistance of less than 1.5 $m\Omega/\square$ and the majority of the lines is patterned as straight lines between the vias and the conductors, respectively.